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TO:	FROM:
Mail Stop Amendment	Trueman H. Denny III, Reg. # 44,652 408-737-7200 @ 124
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USPTO – Examiner Nguyen, Hien N., Art Unit 2824	FEBRUARY 1, 2006
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571-272-1879	PROPOSAL FOR S/N 10/773,549

☐URGENT ☐FOR REVIEW ☐ PLEASE COMMENT ☐ PLEASE REPLY ☐ PLEASE RECYCLE

NOTES/COMMENTS:

Docket #	P038.04	By:	THD3	Faxing Date :	February 1, 2006
Ser. No:	10/773,549	Filing Date:	02/06/2004	Inv(s)	Rinerson et al.
Title:	MULTI-RESISTIVE STATE ELEMENT WITH REACTIVE METAL				

The following is being transmitted to the U.S. Patent Office:

Item	*Description*	*# Pgs*
1.	**Proposal for Amending Drawing(s) in Response to OA mailed on 11/29/2005**	11
2.		
3.		
4.		
5.		
6.		
7.		

S/N 10/773,599 Filed: 02/06/2004

165, and 170 is associated with only one x-direction conductive array line layer and one y-direction conductive array line layer. Although the top conductive array line layer 185 and bottom conductive array line layer 175 are only used to supply voltage to a single memory layer 155 and 170, the other conductive array line layers 180, 190, and 195 can be used to supply voltage to both a top and a bottom memory layer 155, 160, 165, or 170. Co-pending U.S. patent application, "Re-Writable Memory With Multiple Memory Layers," U.S. Application No. 10/612,191, filed July 1, 2003, incorporated herein by reference in its entirety for all purposes, describes stacked cross point arrays.

(5 pt) 273 1879

[0016] Referring back to FIG. 2B, the repeatable cell that makes up the cross point array 100 can be considered to be a memory plug 255, plus 1/2 of the space around the memory plug, plus 1/2 of an x-direction conductive array line 210 and 1/2 of a y-direction conductive array line 215. Of course, 1/2 of a conductive array line is merely a theoretical construct, since a conductive array line would generally be fabricated to the same width, regardless of whether one or both surfaces of the conductive array line was used. Accordingly, the very top and very bottom layers of conductive array lines (which use only one surface) would typically be fabricated to the same size as all other layers of conductive array lines.

[0017] One benefit of the cross point array is that the active circuitry that drives the cross point array 100 or 150 can be placed beneath the cross point array, therefore reducing the footprint required on a semiconductor substrate. Co-pending U.S. patent application, "Layout Of Driver Sets In A Cross Point Memory Array," U.S. Application No. 10/612,733, filed July 1, 2003, incorporated herein by reference in its entirety for all purposes, describes various circuitry that can achieve a small footprint underneath both a single layer cross point array 100 and a stacked cross point array

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